

Five-level one-capacitor boost multilevel inverter

ISSN 1755-4535

Received on 7th January 2020

Revised 25th March 2020

Accepted on 16th April 2020

E-First on 5th June 2020

doi: 10.1049/iet-pel.2020.0033

www.ietdl.org

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Abstract: Multilevel inverter configurations are a suitable candidate for medium and high power applications. This study presents a new one-capacitor-based five-level ($2V_{dc}$, V_{dc} , 0, $-V_{dc}$, $-2V_{dc}$) boost multilevel inverter. The single-phase version of the proposed formation has one dc-source, eight switches and one capacitor. To provide boosting ability, the inverter is operating based on charge-pump theory, where the capacitor is charging in parallel and discharging in series connections to provide a higher output voltage. The proposed configuration requires simple control tasks, and for this purpose, level-shift pulse width modulation strategy, where the reference signal is compared with four carriers, is implemented to drive the switches and generates the required pulses pattern. The developed inverter has some distinct features like the usage of only one dc-source and one-capacitor, compact size, simple control requirements and boosting ability. The system is simulated with MATLAB/Simulink and a hardware prototype is developed to verify the performance of the developed five-level configuration. The results show that the developed five-level multilevel inverter reaches the expected performance

1 Introduction

In renewable energy systems, dc to ac conversion is typically required to generate the ac output with certain amplitude, frequency and small harmonic profile. Pulse width modulation (PWM) inverters with two-level or multilevel configurations are the mainstream ac/dc power electronic interfaces. They enable controlled amplitude, frequency and harmonics of the output voltage. Multilevel inverter configurations generate the ac output with reduced harmonic components. Hence, multilevel inverter topologies were covered extensively in the literature due to their merits such as small filter size and improved output waveform [1–9].

In a multilevel inverter, multiple dc levels are used to synthesise a staircase waveform utilising power semiconductors. In comparison with two-level conventional inverters, multilevel inverters have improved harmonic profile and reduced semiconductor voltage stresses [10].

The power quality of multilevel inverter improves with the increase in levels. On the opposite side, increasing the levels leads to a large number of power semiconductors and associated driving circuitries. Hence, system cost and complexity are high. This affects system reliability and efficiency [10, 11].

Various multilevel inverter configurations were developed. Those configurations include neutral point clamped (NPC), cascaded H-bridge (CHB), flying capacitor (FC) and modular multilevel converters [12–15]. Those multilevel schemes can be configured to generate 3, 5, 7, or n -level output voltage [16].

NPC inverter was introduced by Akira Nabae and Akagi [17], as a three-level diode clamped form for motor drive. Stability and balancing of the dc-capacitors are a big concern of this topology, although it has only one dc-source. As the dc-capacitors are fed by the dc-source, capacitor voltage and current are controlled to keep the stability and balance of the two stacks [18].

Instead of clamping diode, Stillwell and Pilawa-Podgurski [19] used a FC to clamp the voltage of one capacitor voltage-level, which is a FC multilevel converter. FC multilevel inverter owns some distinct feature over the NPC counterpart, which is the phase redundancies. Such feature gives the FC flexibility in charging or discharging, and overcome voltage unbalance or faults. Moreover, redundancy improves voltage stresses across the power switches

and harmonic profile. Meanwhile FC multilevel inverter suffers from different drawbacks such as control complexity to manoeuvre voltage of all capacitors and poor switching efficiency [15, 18].

Another formation of multilevel inverter is the CHB multilevel converter, which is built by series-connected h-bridge inverters. Each bridge has its dc-source. The modularity of this formation gives it an obvious advantage over neutral point and FC configurations, it gives the inverter high flexibility in fault tolerance and low power level operation after cell failure [20].

Scalable technology or modular multilevel inverter is another power configuration of multilevel inverters. Where submodules with independent control systems are connected in cascade formation to generate any number of levels required. However, current circulation within the converter increases the overall conduction losses of the system and balancing the submodule capacitor is the main issue in controlling the modular multilevel topologies [15, 18].

This manuscript presents a new five-level boost inverter. Different five-level configurations are presented in the literature. Five-level formation presented in [21], can generate five-level output with six switches, two diodes and two capacitors. Although it has less number of switches, it requires a complex control algorithm for balancing the capacitors and diodes, deteriorating overall system efficiency. The configuration presented in [22] is similar to the one presented in [21], as it is based on the switched capacitors cell, but designed to generate nine levels instead of five levels. Roy *et al.* [23] developed a cross-switched inverter based on switched-capacitor-converters, it utilises an optimum number of switches, however, its five-level version includes two capacitors, which would lead to more control complexity. Another distinct five-level topology is presented in [24]. However, it requires seven-switches, four-diodes, and two capacitors to generate the required five-level output.

The new proposed configuration is a modification of the multilevel inverter configurations proposed in [25, 26]. Topologies presented in [25, 26] can generate nine-level but requires two dc-sources with different voltage amplitude and in case of three-phase configuration, it requires six dc-sources. On the other hand, the proposed version in this study can generate a five-level output voltage with only one dc-source and one capacitor and in three-phase configuration, still, one dc source is enough to implement the

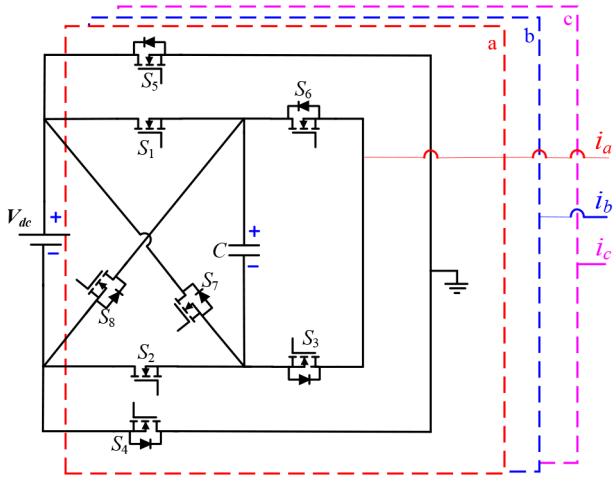


Fig. 1 General Schematic representation of proposed five-level inverter

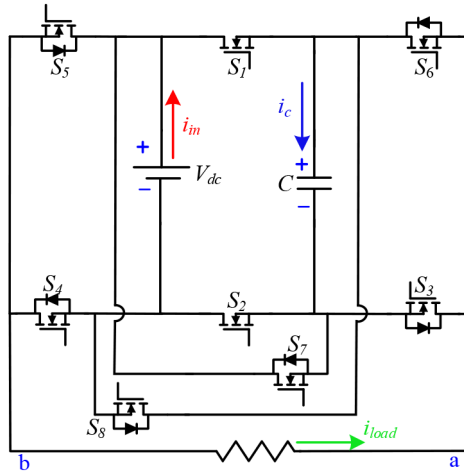


Fig. 2 Single-phase configuration of the proposed five-level inverter

three-phase output voltage. Another advantage of the proposed configuration over its counterpart in [25, 26] is its boosting ability, where the output voltage is higher than twice the input voltage. The proposed configuration generates five-level output voltage with amplitude double of the input voltage using only one dc-source, one-capacitor and eight power switches. Generated output voltage levels are $(2V_{dc}, V_{dc}, 0, -V_{dc}, -2V_{dc})$. The general schematic representation of the proposed system is depicted in Fig. 1. The system can be extended to the three-phase version by using three capacitors, and 24 power switches. In this study only single-phase configuration will be studied and investigated. The capacitor is connected in parallel in some states with the dc-source to be charged. Then it is reconnected to be in series with the dc-source to generate $2V_{dc}$ output voltage level. To drive the switches of the multilevel inverter, level-shift PWM (LS-PWM) is implemented in this study. The reference voltage is compared with four carriers to generate the required switching states.

The study is organised as follows: Section 2 discusses operation modes of the developed multilevel boost-inverter. Section 3 discusses the modulation strategy while Section 4 considers calculation of the losses by the proposed configuration and Section 5 includes simulation and experimental results.

2 Proposed five-level boost multilevel inverter

The proposed five-level boost multilevel inverter is depicted in Fig. 2. The proposed topology is a five-level multilevel inverter with boosting ability and the output voltage is double the input voltage. The developed topology has only eight switches, two of them are without anti-parallel diode. Although the proposed inverter has 2^8 possible switching states, only six valid switching states are implemented, as discussed in Table 1, to generate the

five-level output voltage. All valid operation modes are depicted in Figs. 3 and 4.

2.1 Operation modes

Mode 1, freewheeling occurs: the inverter generates output voltage equal to zero and capacitor C is charging from the dc-source (see Fig. 3a). During this analysis the capacitor is assumed to be charged when the capacitor voltage is zero, large inrush current is drawn. Indeed, most of the multilevel topologies with FCs would suffer from the same concern. In high power applications, a pre-charge device could be adopted, which allows capacitor voltage to build up gradually [27–32]. S_1, S_2, S_3 and S_4 are on, while the other switches are off. Capacitor C is charging from the dc source and has a voltage equal to the dc-source voltage. Capacitor C is charged from the input voltage and its steady-state value equals the input voltage. Output terminal a is connected to output terminal b .

Mode 2: the inverter generates output voltage equals to the input voltage (see Fig. 3b), S_1, S_2, S_3 and S_5 are on, while the other switches are off. Capacitor C is charged from the dc source and has its voltage equal to the dc-source voltage. Output positive terminal b is connected to the positive terminal of the input source, while the terminal a is connected to the negative terminal of the dc-source.

Mode 3: the inverter generates output voltage, which is equal to twice the input voltage (see Fig. 3c), switches S_3, S_5 and S_8 are on, while the other switches are off. Output positive terminal b is connected to the positive terminal of the dc-source, while terminal a is connected to the negative terminal of capacitor C .

Mode 4, freewheeling occurs: the inverter generates output voltage equal to zero and capacitor C is charged from the dc-source (see Fig. 4a). S_1, S_2, S_3 and S_4 are on, while the other switches are off. C is charged from the dc source and has its voltage equal to the dc-source voltage. C is charged from the input voltage and its steady-state value is equal to the input voltage. Output terminal b is connected to output terminal a .

Mode 5: the inverter generates output voltage, which is equal to the input voltage (see Fig. 4b), S_1, S_2, S_4 and S_6 are on, while the other switches are off. C is charging from the dc source and has a voltage equal to the dc-source voltage. Output positive terminal b is connected to the negative terminal of the dc-source, while terminal a is connected to the positive terminal of the dc-source.

Mode 6: the inverter generates output voltage equals to twice the input voltage (see Fig. 4c), S_4, S_6 and S_7 are on, while the other switches are off. Output positive terminal b is connected to the negative terminal of the dc-source, while terminal a is connected to the positive terminal of capacitor C .

2.2 Parameter design

The selection of capacitance is important to ensure lower ripple amount on the capacitor voltage, large ripple in capacitor voltage may cause asymmetry in output voltage steps. According to the analysis in Figs. 3a, b and 4a, C is paralleled with the dc source and is charged. This leads to the following characteristic equations:

$$\{v_c = v_{dc} \Leftrightarrow i_c = i_{in} \quad (1)$$

In mode displayed in Fig. 4a, C is still being charged. However, its current equation is different from the previously mentioned equation and it could be marked as

$$\{v_c = v_{dc} \Leftrightarrow i_c = i_{in} - i_{load} \quad (2)$$

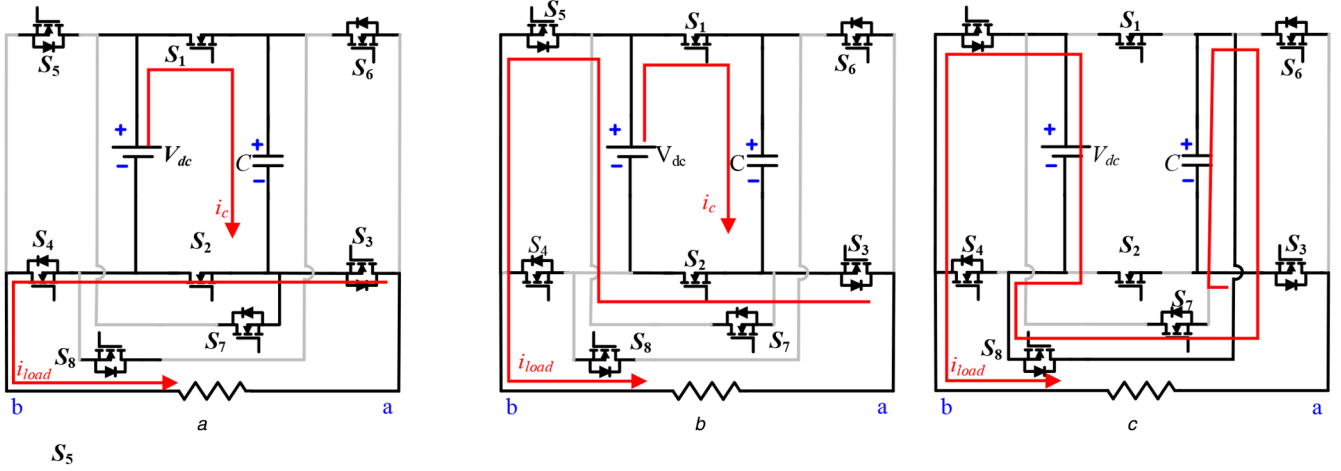
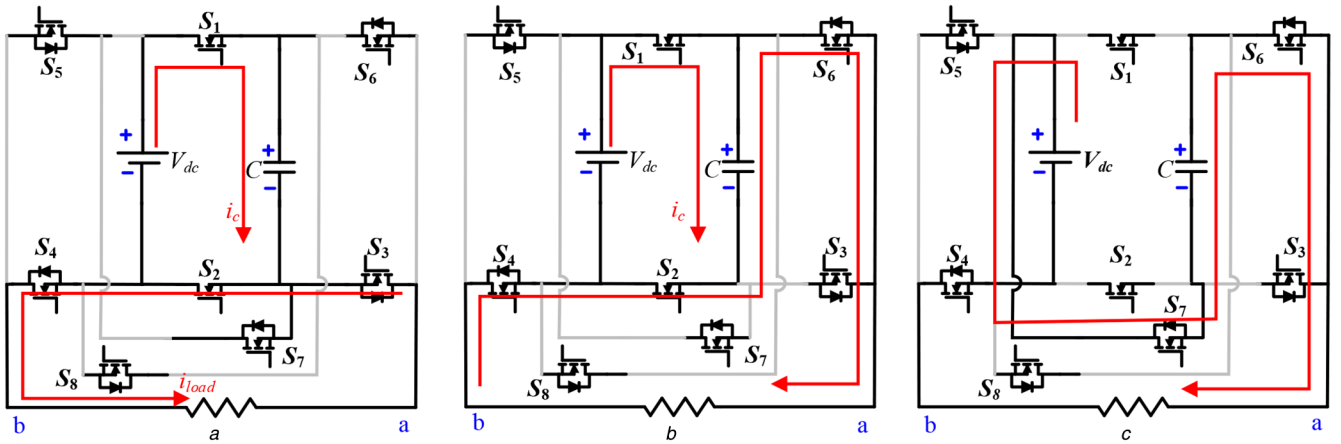
C is discharging in modes described in Figs. 3c and 4b, and capacitor characteristics equation during these modes is

$$\{v_c = v_o - v_{dc} \Leftrightarrow i_c = i_{in} \quad (3)$$

A graph of capacitor voltage is depicted in Fig. 5. From the graph and (1–3), C could be selected as follows:

Table 1 Switching states of the five-level inverter

Vector	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Output
V_0	1	1	1	1	0	0	0	0	0
V_1	1	1	1	0	1	0	0	0	V_{dc}
V_2	0	0	1	0	1	0	0	1	$2V_{dc}$
V_3	1	1	1	1	0	0	0	0	0
V_4	1	1	0	1	0	1	0	0	$-V_{dc}$
V_5	0	0	0	1	0	1	1	0	$-2V_{dc}$

**Fig. 3** Operation modes
(a) Mode I, (b) Mode II, (c) Mode III**Fig. 4** Operation modes
(a) Mode IV, (b) Mode V, (c) Mode VI

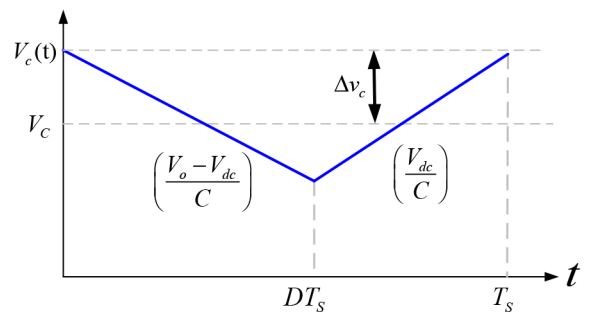
$$C = \left(\frac{v_o - v_{dc}}{2\Delta v_c} \right) DT_s \quad (4)$$

As indicated, C depends on the input voltage v_{dc} , the output voltage v_o , sampling time T_s , accepted amount of ripple in capacitor voltage Δv_c , and the duty ratio D .

The voltage and current stresses of components are summarised in Table 2. All the switching devices have similar current stresses. However, different voltage stresses are observed. S_7 and S_8 exhibit the highest voltage stress, which equals the output voltage. Other switches are having voltage stress equal to the input voltage. It should be noted that due to the circuit asymmetry, the voltage stresses of S_7 and S_8 are higher than that of the other switches. Thus, special attention needs to be paid in component selection.

3 Level shift pulse width modulation

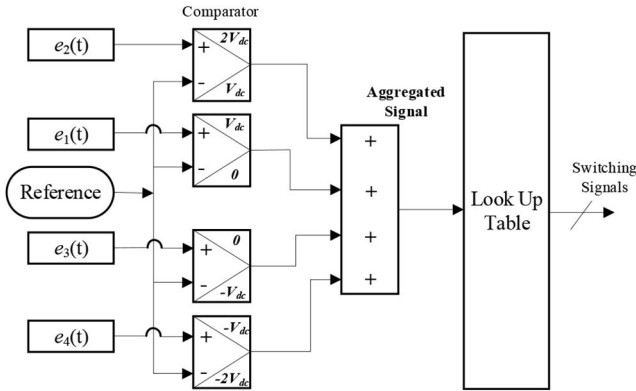
PWM is widely used to drive the switches of power converters (dc or ac converters) at a given switching frequency. Pulses pattern

**Fig. 5** Capacitor voltage illustration

generated by the PWM block is implemented in a way to give a higher modulation index and less harmonic profile of the output waveform. Moreover, modulation schemes can be designed to reduce switching losses, current ripple, and balance capacitor voltage. In the two-level converter, a single triangular carrier is compared with the modulation signal to develop the switching

Table 2 Devices voltage and current stress

Device	Voltage stress	Current stress
S ₁	V _{in}	I _{in}
S ₂	V _{in}	I _{in}
S ₃	V _{in}	I _{in}
S ₄	V _{in}	I _{in}
S ₅	V _{in}	I _{in}
S ₆	V _{in}	I _{in}
S ₇	V _o	I _{in}
S ₈	V _o	I _{in}

**Fig. 6** Switching signal generation schematic diagram

pattern of the switches. To extend a similar technique with multilevel topologies, the phase-modulated signal is compared with multiple triangular carriers. According to carrier arrangement, multicarrier modulation is divided into the phase-shifted PWM carrier and LS-PWM carrier.

In this study, LS-PWM is generated to control the five-level inverter proposed in this study. The general schematic representation for generating switching signals for the inverter switches are depicted in Fig. 6. According to [33], N -level inverter requires $(N-1)$ carrier waveforms and a reference signal. As the proposed topology has five-level, four-carriers are employed as depicted in Fig. 7. The switching pattern is determined by comparing the carrier signals with a sinusoidal reference waveform. The four-carriers are symmetrical with the same amplitude, same phase shift and switching frequency.

The modulation procedure represents four different sectors. In sector 1, the reference signal is compared with carrier signal e_3 and generates output voltage from zero to $-V_{dc}$. In sector 2, the reference signal is compared with carrier signal e_4 and generates output voltage from $-V_{dc}$ to $-2V_{dc}$. Due to the symmetrical operation of the proposed seven-level boost converter. The positive half cycle is illustrated with the same procedure.

The switching patterns of the multilevel inverter are depicted in Fig. 8.

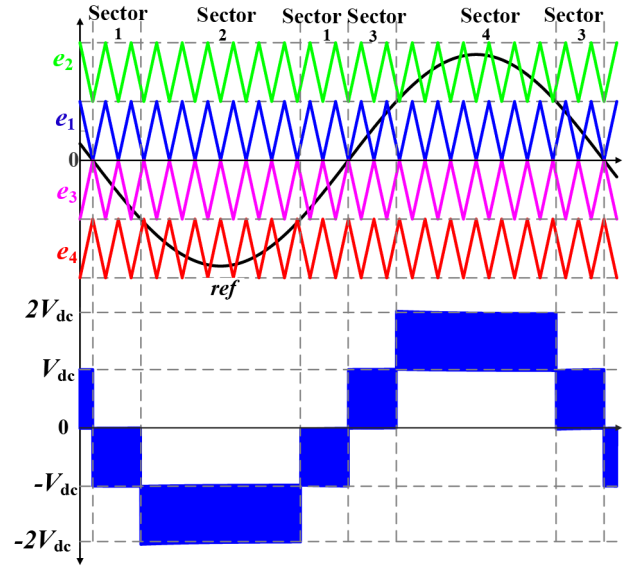
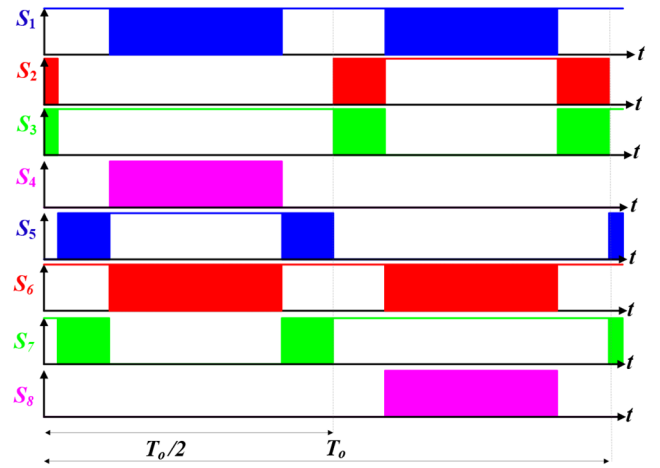
4 Loss analysis

Each switching device incurs two types of losses; conduction losses when the device is conducting and switching losses when the device is switching (change state from off to on and vice versa).

In each switching state, of the eight possible states, at least three switches are turned on or switched to be on. This leads to two types of losses, conduction losses and switching losses. In the upcoming sections, analytical calculation for the switching and conduction losses is discussed.

4.1 Conduction losses

The proposed topology has eight switches, two of its power switches and unidirectional conducting and blocking while the remaining six switches are unidirectional blocking and

**Fig. 7** LS-PWM scheme**Fig. 8** Driving signals of the five-level inverter

bidirectional conducting, the instantaneous conduction losses of the power switch and its body diode can be given as [14, 24]

$$\rho_{c,T}(t) = [V_T + R_T i^\alpha(t)] i(t) \quad (5)$$

$$\rho_{c,D}(t) = [V_D + R_D i(t)] i(t) \quad (6)$$

The average conduction losses are expressed as

$$\rho_{c,avg} = \frac{1}{\Pi} \int_0^\Pi \left[\{N_T(t)V_T + N_D(t)V_D\} i_L(t) + \{N_T(t)R_T i_L^{\alpha+1}(t) + \{N_D(t)R_D i_L(t)\} \right] d(\omega t) \quad (7)$$

where $\rho_{c,T}(t)$, $\rho_{c,D}(t)$, V_T , V_D , R_T , R_D , α , N_D , N_T and $\rho_{c,avg}(t)$ denote the instantaneous conduction losses of the transistor, the instantaneous conduction losses of the diode, transistor on-state voltage drop, diode instantaneous voltage drop, transistor equivalent on-resistance, diode equivalent on-state resistance, constant given by transistor characteristics, number of conducting diodes, number of conducting transistor and average conduction losses, respectively.

4.2 Switching losses

Switching losses of each switching device can be estimated using a linear approximation of voltage and current during the switching period, [14, 24]. Turn-on energy losses can be calculated as

$$E_{on,j} = \int_0^{t_{on}} \left\{ \left[V_{o,j} \frac{t}{t_{on}} \right] \left[-\frac{I}{t_{on}}(t - t_{on}) \right] \right\} dt = \frac{1}{6} V_{o,j} I t_{on} \quad (8)$$

Similarly, energy losses of the j th switch during turning off are calculated as

$$E_{off,j} = \int_0^{t_{off}} \left\{ \left[V_{o,j} * \frac{t}{t_{off}} \right] \left[-\frac{I}{t_{off}}(t - t_{off}) \right] \right\} dt = \frac{1}{6} V_{o,j} I t_{off} \quad (9)$$

where $E_{on,j}$, t_{on} , I , $V_{o,j}$, $E_{off,j}$ and t_{off} denote to turn-on loss of the j th switch, turn-on time, current through the switch after turning on, voltage of the j th switch during turning off, turn-off loss of the j th switch, and turn-off time, respectively.

Total switching power losses can be calculated as:

$$\rho_s = \sum_{j=1}^{2n+2} \left[\frac{1}{6} V_{o,j} * I(t_{on} + t_{off}) f_j \right] \quad (10)$$

A graph of the inverter efficiency is depicted in Fig. 9. The optimum operating power range for the proposed inverter is between 350 and 650 W. However, in all power range up to 800 W, its efficiency is >95%.

5 Results and discussions

For validating the operation at different scenarios, the system is simulated in MATLAB/Simulink and a hardware prototype is built in the laboratory.

5.1 Simulation results

During the simulation, the input voltage is fixed at 200 V, while switching frequency is fixed to 5 kHz. Different cases of studies have been studies in the simulation platform. Relation between input current and capacitor current is depicted in Fig. 10. It should be noted that each time the capacitor C is charged, an inrush charging current occurs. This phenomenon can be observed in Fig. 10. Therefore, the proposed topology fits better for low power applications.

The proposed topology has only one capacitor and one dc-source, this gives an obvious advantage over different topologies in the literature, as no balancing control is required. In Fig. 11, the resistive load is connected to the inverter without any output filter. Output voltage, as well as output current has five-level (0, v_{dc} , $2v_{dc}$, $-v_{dc}$, $-2v_{dc}$). Total harmonic distortion (THD) in this case of study, as illustrated in Fig. 12, is found to be around 34%. After adding a filter this value could be reduced to standard value with small filter size compared to two-level or three-level configurations.

Fig. 13 demonstrates the case study where an inductive load is connected to the inverter terminals. Similar to the resistive load scenario, there is no output filter used, but the output current is smoothed due to the inductive load. THD of the output current is around 5.14%, as can be seen in Fig. 14.

5.2 Experimental results

The general schematic representation of the implemented hardware configuration is illustrated in Fig. 15a and photocopy of the implemented system is illustrated in Fig. 15b. DSPace 1202 is used to implement the LS-PWM and hence generate the gating signals for the power switches. Eight IRFP264 power MOSFETs are used to implement the five-level multilevel inverter.

Fig. 16 is a case of study where the resistive load is connected to the terminal of the inverter and input voltage raised to 60 V. Generated voltage is around 120 V. Fast Fourier transform of the measured output current with resistive load is captured in Fig. 17, which is used to calculate the THD of the output current. According to Fig. 17, THD is <25% without adding filter.

Fig. 18 captures the experimental waveforms of the prototype with an L - R load. No filter is added. The inductive load helps to

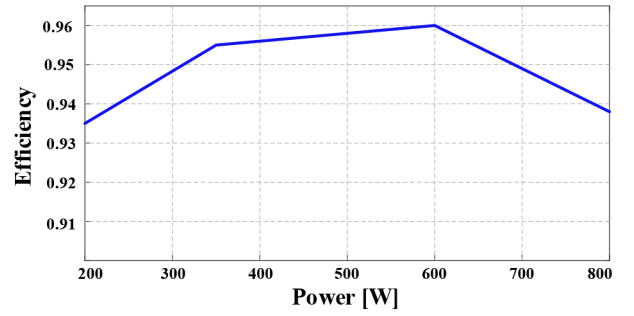


Fig. 9 Estimated efficiency of the proposed five-level multilevel inverter

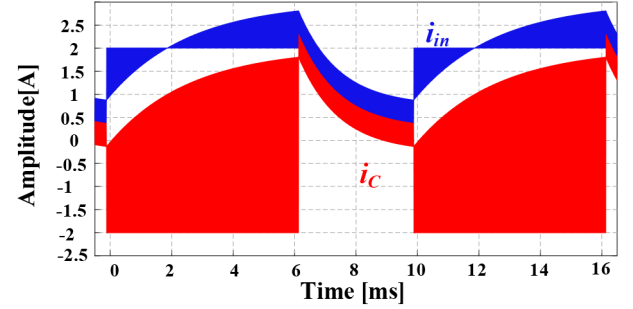


Fig. 10 Characteristics of input current and capacitor current

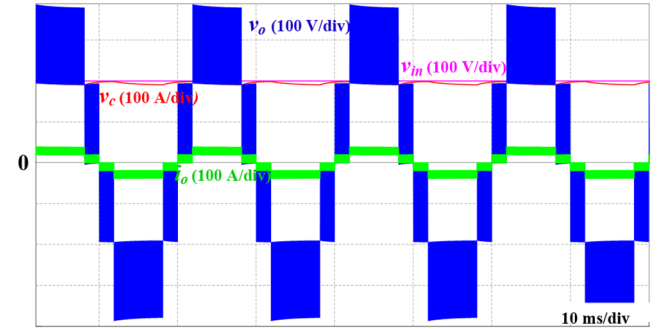


Fig. 11 Output voltage, output current, input voltage and capacitor voltage, with resistive load, $R = 200 \Omega$

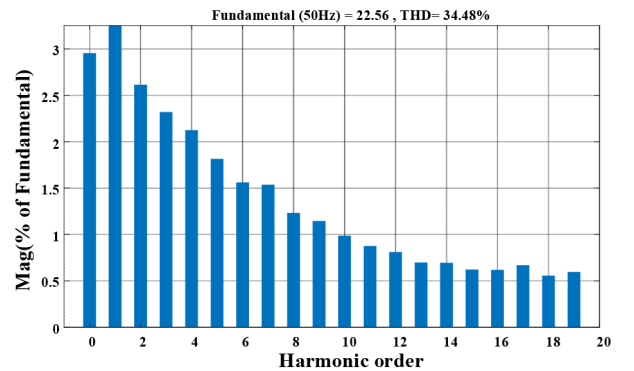


Fig. 12 THD of output current with resistive load and no filter is added

suppress the current harmonics. Correspondingly, the THD of the output current is reduced to 8%.

Comparison between the proposed five-level boost inverter and different five-level topologies existing in the literature is depicted in Table 3. NPC would require eight power switches and five capacitors and still no boosting ability, which means the output voltage is lower than input voltage. FC five-level inverter has similar components count as NPC, but with three capacitors instead of five. CHB inverter, has no capacitors but require a large number of independent dc-sources. As a conclusion from the table, the proposed configuration can generate five-level output with boosting ability, the output voltage is double the input voltage, and with the minimum number of component counts.

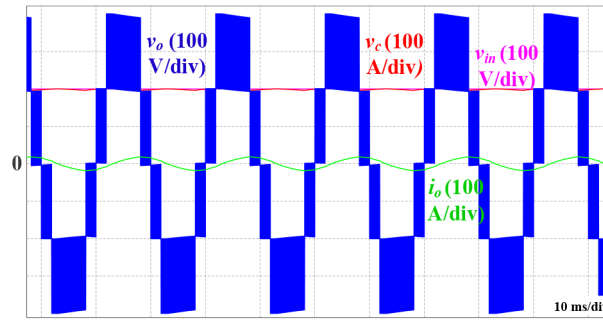


Fig. 13 Output voltage, output current, input voltage and capacitor voltage, with inductive load, $R = 10 \Omega$ and $L = 5 \text{ mH}$

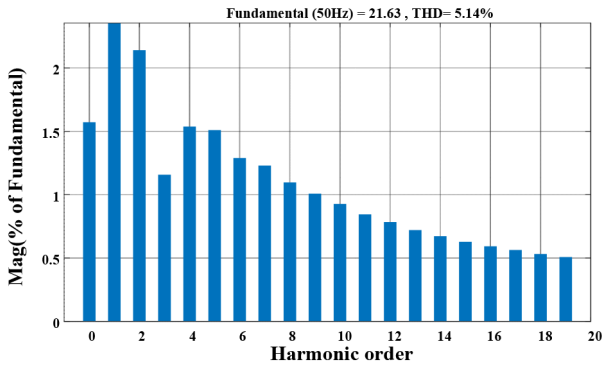


Fig. 14 THD of output current with inductive load and no filter is added

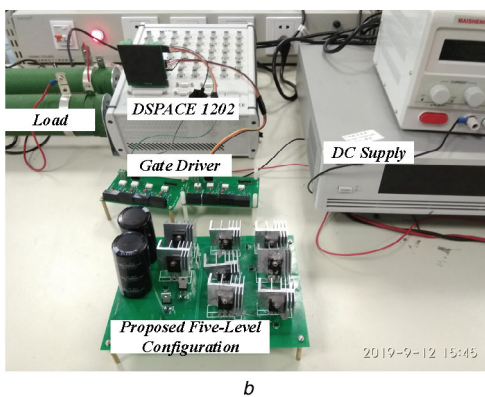
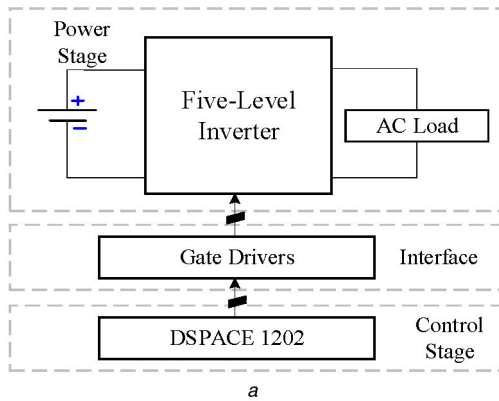


Fig. 15 Experimental setup
(a) Block diagram, (b) Photograph of prototype

6 Conclusion

This study presented a five-level boost multilevel inverter. The developed configuration, constructed from eight switches and only one dc-capacitor, for a single-phase version. It can generate a five-level output with an amplitude higher than twice the input voltage. As only one capacitor is utilised in this configuration, the balancing problem is not the issue in this configuration.

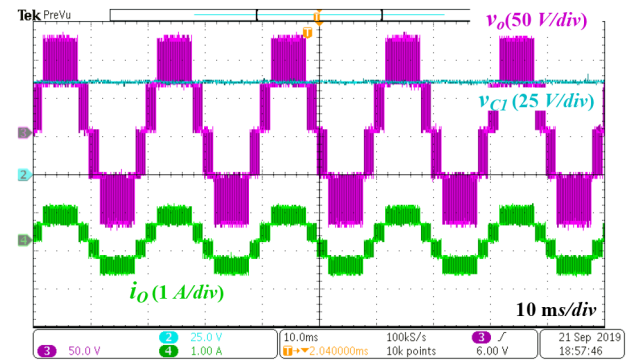


Fig. 16 Measured output voltage, output current and capacitor voltage with resistive load and no output filter, $R = 50 \Omega$

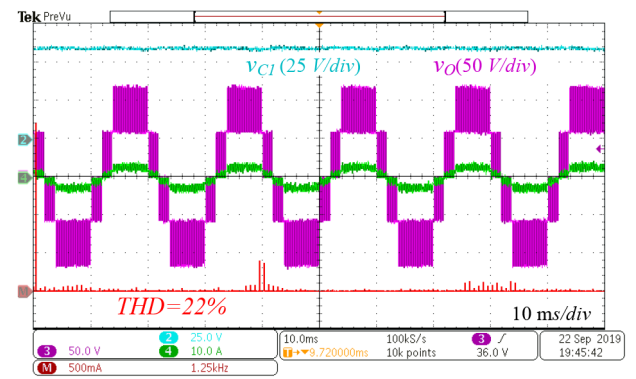


Fig. 17 Measured THD, output voltage, output current and capacitor voltage with resistive load and no output filter $R = 50 \Omega$

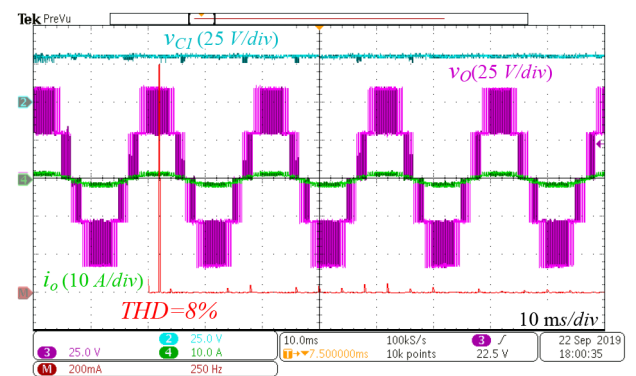


Fig. 18 Measured THD, output voltage, output current and capacitor voltage with inductive load and no output filter, $R = 10 \Omega$ and $L = 3 \text{ mH}$

The boosting feature of the proposed inverter makes it a competitive counterpart for PV system applications. The dc-capacitor is charged from the dc-source, and then it is reconfigured to be series with the dc-source. Hence higher output voltage can be obtained. To drive switches of the inverter, LS-PWM is applied. Switching states are designed to ensure sufficient charging period for the capacitor, and hence no big ripple in the capacitor voltage.

Table 3 Component requirements for single-phase five-level multilevel inverter

Topology	NPC [34]	FC [19]	CHB [35]	[10]	[36]	Diode clamped [37]	Capacitor clamped [38]	This work
number of main switches	8	8	8	4	5	8	12	8
number of diodes	0	0	0	4	4	6	0	2
number capacitors	3	3	0	2	2	4	4	1
number of dc-source	1	1	2	1	1	1	1	1

For verification and validation of the introduced system, it is simulated in MATLAB/SIMULINK platform and a hardware prototype is implemented in the laboratory. Results obtained from simulation and experimental results are consistent and agree with the analytical analysis.

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